



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,398	12/12/2003	Ronald C. Meadows	5308-376	1180
20792 7590 01/18/2007 MYERS BIGEL SIBLEY & SAJOVEC PO BOX 37428 RALEIGH, NC 27627			EXAMINER	
			MAI, ANH D	
			ART UNIT	PAPER NUMBER
			2814	
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	01/18/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/734,398	MEADOWS, RONALD C.	
	Examiner Anh D. Mai	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 27 December 2006.

2a)  This action is FINAL.                            2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 1,4-8,10-20 and 28-30 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1,4-8,10-20 and 28-30 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892) 4)  Interview Summary (PTO-413)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date. \_\_\_\_.  
3)  Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 5)  Notice of Informal Patent Application  
6)  Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 27, 2006 has been entered.

### ***Status of the Claims***

2. The Remarks and Declaration under 37 C.F.R. § 1.131, filed December 27, 2006 have been entered. Claims 1, 4-8, 10-20 and 28-30 are pending.

### ***Claim Objections***

3. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 28 (the second occurrent) and 29 have been renumbered claims 29 and 30.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 4-8, 10-20 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morse (U.S. Patent No. 6,534,857), in view of Palmour (U.S. Patent No. 5,270,554) all of record.

With respect to claim 1, Morse teaches a semiconductor device substantially as claimed including:

a plurality of unit cells (24<sub>1-n</sub>) connected in parallel, the unit cells (24) each having a gate finger (24), wherein a pitch between the gate fingers (24) is varied in a predetermined pattern between the gate fingers (24) so as to provide a non-uniform pitch between the gate fingers (24), wherein the predetermined pattern of non-uniform pitch between the gate fingers (24) provides substantially uniform junction temperature to a substantial majority of the gate fingers (24) during high frequency operation. (See Figs. 7-8).

Morse further teaches the invention is related to semiconductor device, particularly, a high frequency FET power cell.

Thus, Morse is shown to teach all the features of the claim with the exception of explicitly indicating the high frequency FET cell are RF.

However, Palmour teaches a similar plurality of unit cells connected in parallel operate at high frequency out put of MHz and GHz, hence RF.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to conclude that the semiconductor device, high frequency FET power cell of Morse is an RF power device.

Regarding the "junction temperature", since the junction is within the substrate, a measurement of the substrate temperature is indirectly measure the junction temperature, thus, the limitation is met.

Note that, the term *during RF operation* is determined as intended use of the product.

With respect to claim 4, the predetermined pattern of non-uniform pitch between the gate fingers (24<sub>1-n</sub>) of Morse provides a substantially uniform junction temperature to all but the outermost gate fingers (24<sub>n</sub>) of the device when in operation. (See Fig. 8).

With respect to claim 5, the unit cells (50) of Morse comprise a plurality of unit cells arranged in a linear array.

With respect to claim 6, the unit cells (50) of Morse comprise a plurality of unit cells arranged in a two dimensional array and the non-uniform pitch gate fingers (24) are provided in at least one of the two dimensions of the two dimensional array.

With respect to claim 7, the non-uniform pitch gate fingers (24) of Morse are provided in both dimensions of the two dimensions of the two dimensional array.

With respect to claim 8, the pitch between the gate fingers (24) varies in a substantially linear pattern from a small pitch to a larger pitch toward the center of the device.

With respect to claim 10, the unit cells of Morse and Palmour comprise MESFET unit cells.

With respect to claim 11, the unit cells of Morse comprise silicon carbide semiconductor device unit cells.

With respect to claim 12, the predetermined pattern of non-uniform pitch between the gate fingers (24) of Morse provides a more uniform junction temperature than a corresponding uniform gate pitch device for a particular set of operating conditions.

With respect to claims 13 and 14, the junction temperature of Morse does not differ by more than about 5 °C over at least 80% or 90% of the plurality of unit cells. (See Fig. 8).

With respect to claim 15, Morse teaches a field effect transistor substantially as claimed including:

a plurality of unit cells (24<sub>1-n</sub>) electrically connected in parallel, each unit cell (24) having a source region (20) and a drain region (22); (see Fig. 1); and

a plurality of gates (24) of the unit cells (24<sub>1-n</sub>), the plurality of gates (24) being electrically connected in parallel and having a non-uniform spacing between the gates (24), wherein the non-uniform spacing between the gates is provided in a pattern that provides a lower peak junction temperature during a high frequency operation than a corresponding uniform gate pitch device for a particular set of operating conditions. (See Figs. 5-8).

Regarding the RF operation and junction temperature, a similar reason as that of claim 1 also applies.

With respect to claim 16, the plurality of unit cells of Morse comprises a linear array of unit cells.

With respect to claim 17, the plurality of unit cells of Morse comprises a two dimensional array of unit cells.

With respect to claim 18, the non-uniform spacing of the gates (24) of Morse is in a single dimension of the two dimensional array.

With respect to claim 19, the non-uniform spacing of the gates (24) of Morse is in both dimensions of the two dimensional array.

With respect to claim 20, the plurality of unit cells of Morse comprises a plurality of silicon carbide unit cells.

With respect to claims 28 and 29, Morse teaches: a non-uniform unit cells having pitch (spacing) of 38, 30, 22 and 13  $\mu\text{m}$ .

Thus, Morse is shown to teach all the features of the claim with the exception of specifically disclosing a larger spacing and a RF output power. Note that, the claimed dimensions and output powers do not appear to be critical.

However, Morse also teaches: while such dimension are not necessarily optimum, they are easily implementable.

Note that the specification contains no disclosure of either the *critical nature of the claimed dimensions or output powers* of any unexpected results arising therefrom. Where

patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum dimensions (larger spacing) of the unit cells as taught by Morse. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to the FETs of Morse to have larger spacing since Morse teaches that spacing is easily implemented, hence optimized.

Further, Palmour teaches an RF operated at an output power of 630 W, 158 W and 45W is obtainable.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to operate the power FET of Morse at the output power as taught by Palmour since an output power as high as 630 W can be easily obtainable.

With respect to claim 30, the spacing between the gates (24) of Morse varies in a substantially linear pattern from a small pitch (ends) to a larger pitch (52) toward the center of the device.

***Response to Arguments***

5. The Declaration filed on December 27, 2006 under 37 CFR 1.131 has been considered but is ineffective to overcome the applied reference.
6. The Morse '857 reference is a U.S. patent or U.S. patent application publication of a pending or patented application that claims the rejected invention. An affidavit or declaration is inappropriate under 37 CFR 1.131(a) when the **reference is claiming the same patentable invention, see MPEP § 2306.** If the reference and this application are not commonly owned, the reference can only be overcome by establishing priority of invention through interference proceedings. See MPEP Chapter 2300 for information on initiating interference proceedings. If the reference and this application are commonly owned, the reference may be disqualified as prior art by an affidavit or declaration under 37 CFR 1.130. See MPEP § 718.

In the Remarks, Applicant states:

Applicant notes that the pending Claims were not rejected on Morse alone, but were **rejected on a combination** of Morse and U.S. Patent No. 5,270,554 to Palmour ("Palmour").

However, the "rejected on a combination" means **rendered obvious** or the same patentable invention.

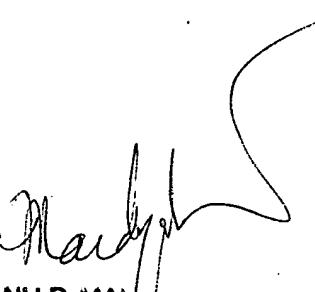
Therefore, the prior invention has not been established or the Declaration under 37 CFR 1.131 is ineffective to overcome the applied references.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



ANH D. MAI  
PRIMARY EXAMINER